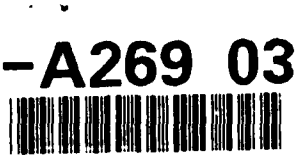


(2) R.L.

QUARTERLY REPORT NO. 8
FOR
ANALOG-TO-DIGITAL CONVERTER
CONTRACT NO. N00014-87-C-0314
1 JANUARY 1989 - 31 MARCH 1989

ARPA Order Number:	9117
Program Code Number:	7220
Amount of Contract:	$2,804,271
Name of Contractor:	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655936, M.S. 105 Dallas, Texas 75265
Effective Date of Contract:	30 March 1987
Contract Expiration Date:	28 February 1990
Contract No.:	N00014-87-C-0314
Program Manager:	W.R. Wisseman (214) 995-2451
Principal Investigator:	Frank Morris (214) 995-6392
Short Title of Work:	GaAs A-to-D Converter
Contract Period Covered by Report:	1 January 1989 - 31 March 1989

20 April 1989

QUARTERLY REPORT NO. 8

FOR

ANALOG-TO-DIGITAL CONVERTER

Contract No. N00014-87-C-0314

1 January 1989 - 31 March 1989

I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high-sampling-rate A/D converter and a high-resolution GaAs A/D converter.

B. ADC Progress

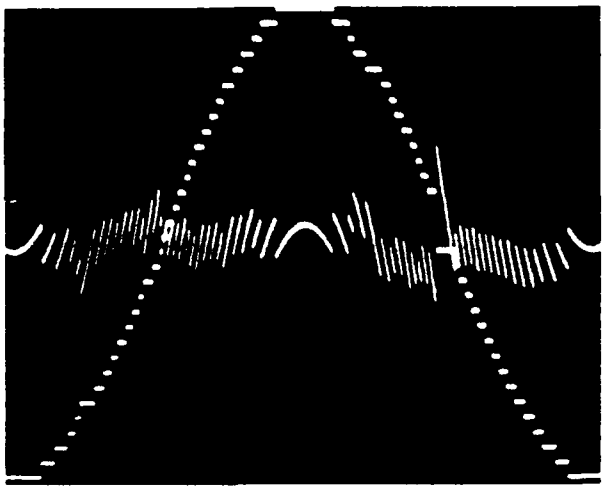
The world's first reported GaAs 5-bit analog-to-digital converters (ADCs) successfully fabricated during 4Q88 have been characterized during the past quarter. Two 5-bit ADC chips from one wafer were packaged in a specially designed hybrid package and tested by Hughes up to a maximum clock frequency of 400 MHz. These 5-bit ADCs, which are building blocks for the radiation-hard monolithic 12-bit ADC to be fabricated for SDIO, exhibited excellent signal-to-noise ratios and linearities. Process improvements have been identified and implemented to reduce the heterojunction bipolar transistor (HBT) junction capacitances to increase the maximum sampling frequency to greater than 1 GHz for the 5-bit ADC design.

The core circuits of the 12-bit ADC, which include a sample-and-hold circuit, gain-switched amplifier, 8-bit digital-to-analog converter (DAC), and an improved 5-bit ADC, have been designed by Hughes and a new mask set will be released in April. A complete 12-bit ADC design is scheduled for release in September 1989.

II. CIRCUIT DESIGN/TESTING PROGRESS

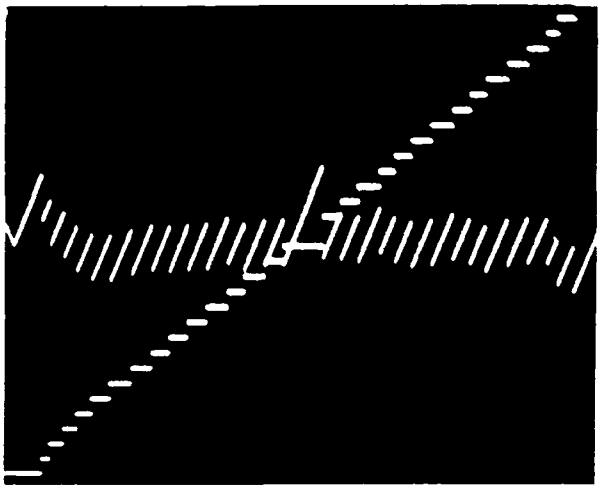
Dynamic characterization of the first lot of functional 5-bit and 4-bit ADCs was completed this quarter. Representative functional die from wafer 107-D were mounted in custom thin-film test hybrids and subsequently evaluated. Signal-to-noise ratio (SNR) performance for the 5-bit ADC (Figure 1) was 26.3 dB (4.1 effective bits) with a sample rate of 400 MHz and

(a) HBT 5-Bit Dynamic Performance



Beat Frequency Test

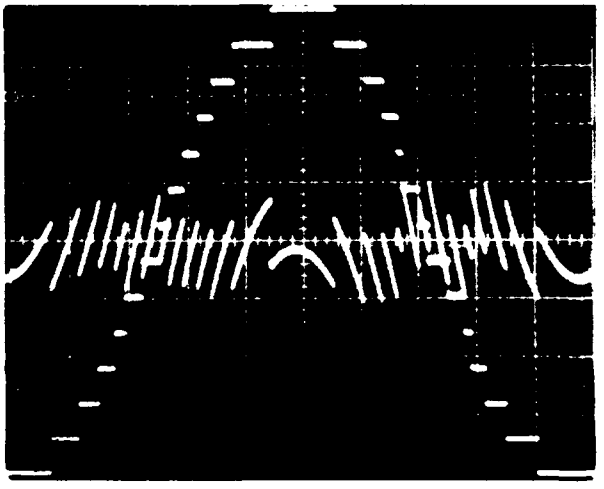
F_{clock} = 400 MHz
F_{video} = 100.001 MHz
SNR = 26.3 dB
Effective Bits = 4.1



1-kHz Ramp Test

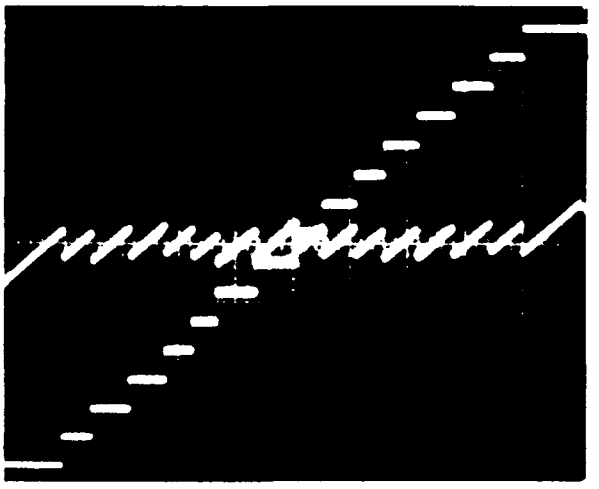
F_{clock} = 400 MHz
F_{video} = 1 kHz
SNR = 20 mV
Linearity = 5 bits, Q (20mV) Untrimmed

(b) HBT 4-Bit Dynamic Performance



Beat Frequency Test

F_{clock} = 350 MHz
F_{video} = 350.001 MHz
SNR = 23.5 dB
Effective Bits = 3.6



1-kHz Ramp Test

F_{clock} = 350 MHz
F_{video} = 1 kHz
Q-level = 40 mV
Linearity = 6 bits, Q/4 (10 mV) Untrimmed

Figure 1. Dynamic performance of HBT 5-bit and 4-bit ADCs.

an input video rate of 100.001 MHz. Similarly, SNR performance for the 4-bit ADC was 23.5 dB (3.6 effective bits) with a sample rate of 350 MHz and an input video rate of 350.001 MHz. Performance of both the 5-bit and 4-bit ADCs compares favorably with the theoretical SNRs of 31.9 dB and 25.8 dB.

A beat frequency technique was used to accurately determine the SNR performance of the HBT ADCs in real time. The sinewave beat frequency test requires that the sample clock (f_c) and the input video signal (f_s) be related by $f_s = f_c/N + \Delta f$, where N is an integer and Δf is a small delta (beat) frequency. In our tests, Δf = 1 kHz. A low-speed, accurate DAC transforms the divided-down ADC digital data back into the analog domain for observation on an oscilloscope display. The DAC output is also applied to a 1-kHz active filter/analog summation circuit. This circuit isolates the 1-kHz fundamental frequency of the DAC output and subtracts it from the unfiltered DAC output to produce a residue waveform. SNR is then determined by comparing the rms power of the filtered fundamental to the rms power of the residue.

Computer simulations completed during the design phase of the 5-bit and 4-bit ADCs predicted a maximum clock rate between 900 MHz and 1.2 GHz for both designs, which is a factor of 2.5 faster than measured performance. A brief device modeling effort, completed this quarter, indicates that the HBT devices fabricated on lot 107 differ significantly from the model used in the 5-bit and 4-bit designs. Computer simulations performed with the updated models predict a maximum ADC clock frequency of 380 MHz, which closely approximates the measured ADC performance.

The results of a Hughes HBT device characterization effort are summarized in Table 1. Measured device parameters for a 7 x 7 μm^2 emitter double-base device are presented. Two parameters strongly linked to the ADC performance, C_{jc} and r_c, differ significantly from the preliminary model used in the 5-bit and 4-bit ADC designs. To produce a 12-bit 20Msps/W ADC and extend the performance of the 5-bit ADC, significant improvements in C_{jc}, r_c, and current gain (β) must be realized. Toward that goal, an improved 5 x 5 μm^2 transistor has been designed by TI (Table 1) and will be used in the design of the 12-bit ADC.

Table 1
Measured HBT 7 x 7 μm^2 Transistor Device Parameters, with Comparison to Projected 5 x 5 μm^2 Device and 12-bit/20-Msps Requirements

HBT Device Parameter	Measured 1/89	Proposed 3/89 2-3 W 12-bit/ 20 Msps ADC	Target Values for 20 Msps/W 12-bit ADC
Emitter Size	7 μm x 7 μm	5 μm x 5 μm	5 μm x 5 μm
C_{jco}	170 fF	30 fF	20 fF
C_{jeo}	70.5 fF	32.5 fF	15 fF
R_e	10 Ω	27 Ω	50 Ω
r_c	536 Ω	51 Ω	70 Ω
R_b	-	584 Ω	500 Ω
T_f	-	2 ps	2 ps
β vs IE	20 @ 1 mA	50 @ 250 μA	50 @ 100 μA

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Also this quarter, a statistical analysis of differential pair V_{be} and β match was completed. The results are presented in Figure 2. For a 7 x 7 μm^2 emitter device at 1 mA, one sigma V_{be} match was 1.2 mV and one-sigma β match was 5%. In comparison, these results equal the matching obtainable with most silicon technologies. The inherent matching of the HBT differential pairs translates directly to the excellent linearity of the 4-bit and 5-bit quantizers.

System-level design of the 12-bit ADC continued. A three-pass 4/5/5 feedback architecture has been identified as the optimal architecture to meet the 20-Msps/W design goal. A block diagram of the 12-bit ADC is shown in Figure 3. Conversion of the input signal to 12 bits is completed with one 4-bit and two 5-bit subconversion cycles. An error-budget analysis was completed to determine the performance requirements of each of the main analog components: sample-and hold (S/H), DAC, 5-bit quantizer, and gain-switch amplifier.

Detailed computer simulation of the S/H, gain-switch amplifier, and 8-bit DAC was begun. To verify the simulated performance of the 12-bit ADC high-resolution components, preliminary versions of the S/H and gain-switch amplifier cores will be released for fabrication in April. Wafer-level performance data including functional yield, amplifier loop gain, bandwidth, offset, and linearity will be available in August. Information gained from S/H and gain-switch test cell evaluation will be incorporated in the complete 12-bit ADC design scheduled for mask release in September 1989.

In addition, the core cells of a 4-bit all-BJT DAC and an 8-bit JFET DAC have been designed and layout captured for fabrication on the April 12-bit test bar. DC linearity and yield analysis of each DAC approach will allow selection of the lowest-risk, highest-performance circuit for the final 12-bit ADC design. Finally, a 5 x 5 μm^2 version of the 400-MHz, 7 x 7 μm^2 5-bit ADC has been captured for release on the April bar. Only minor metal

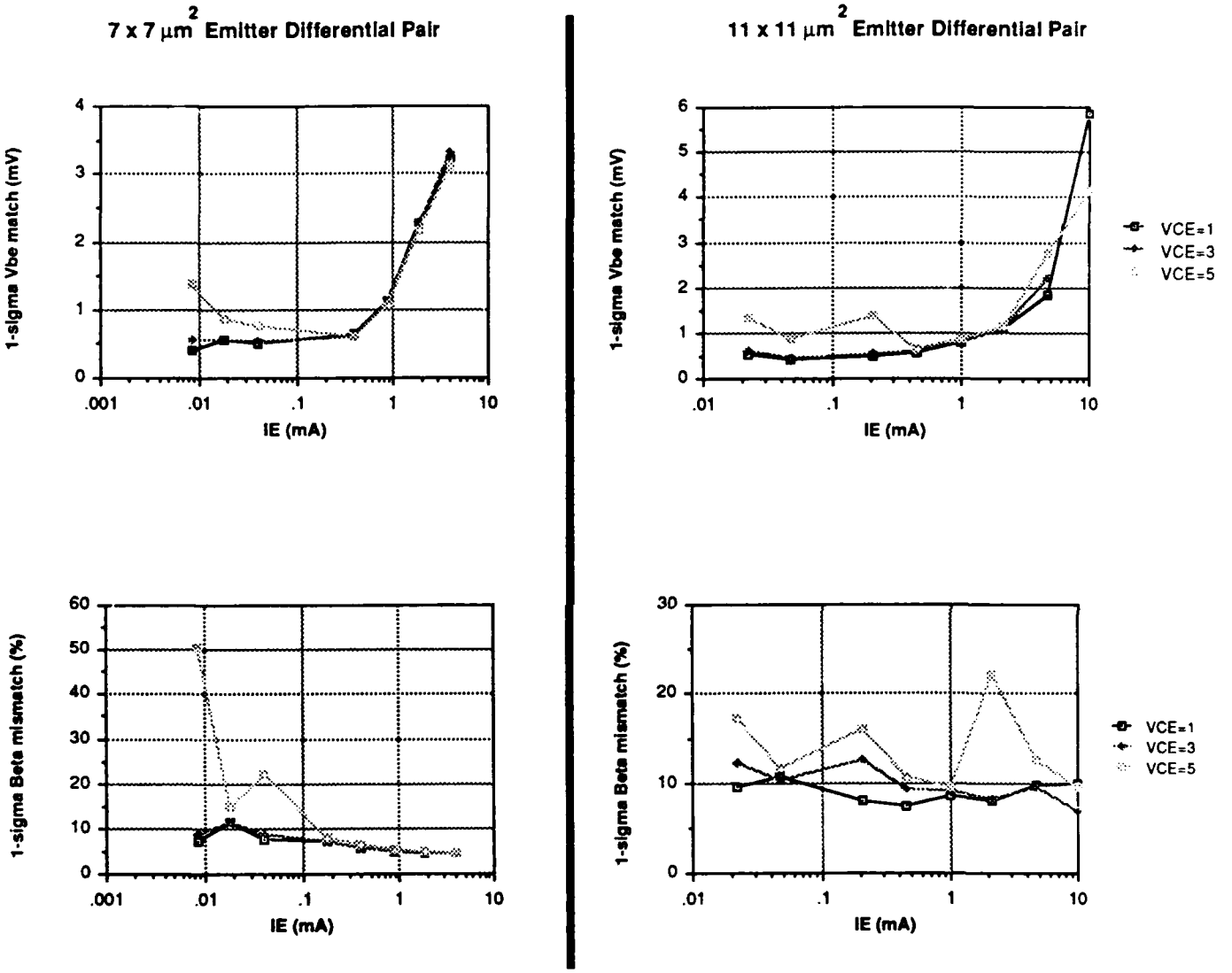


Figure 2. HBT differential pair V_{be} and Beta (β) match measurements (Lot 107-C, -E).

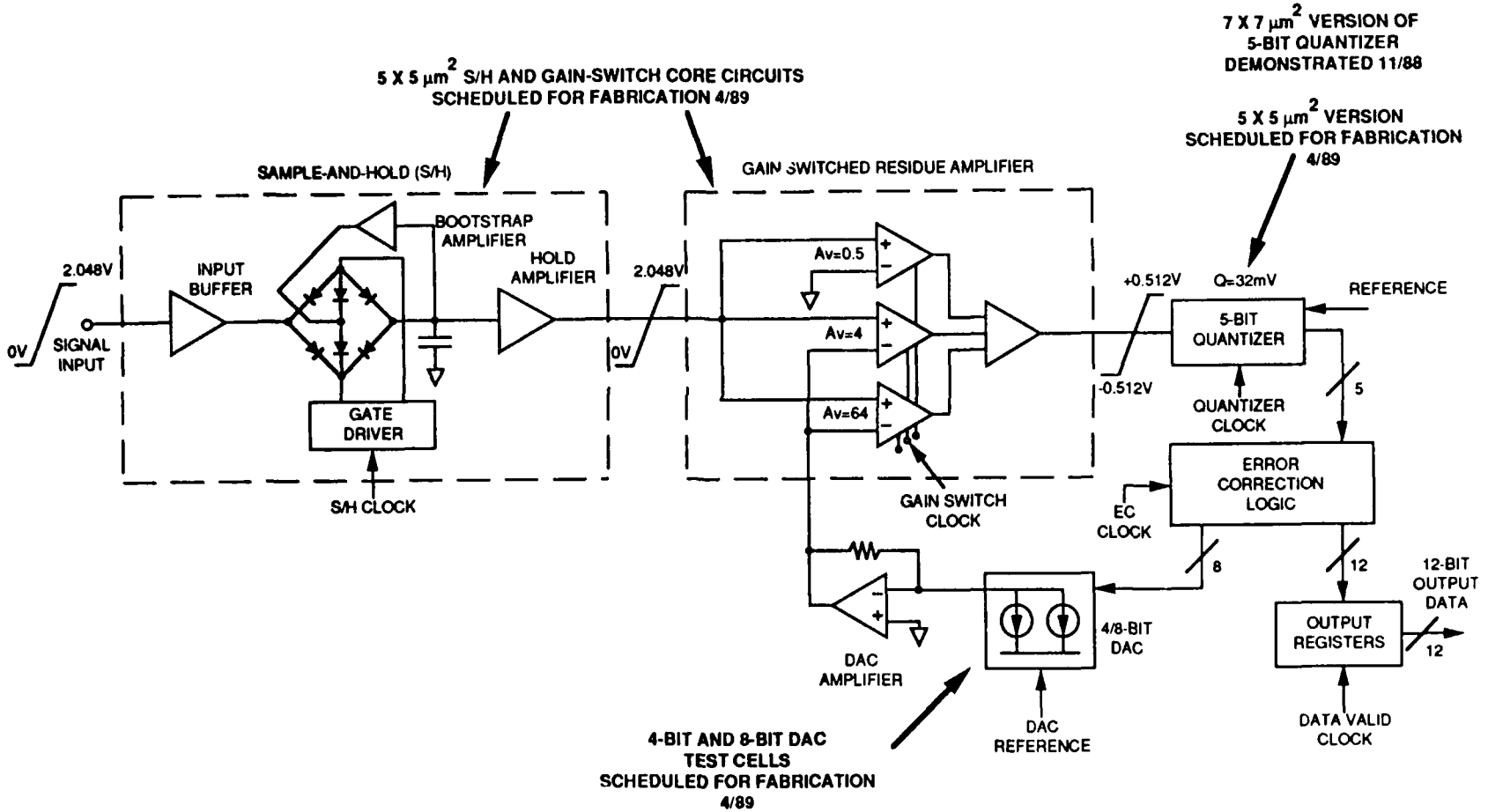


Figure 3. HBT 12-bit 4/5/5 series parallel feedback ADC block diagram.

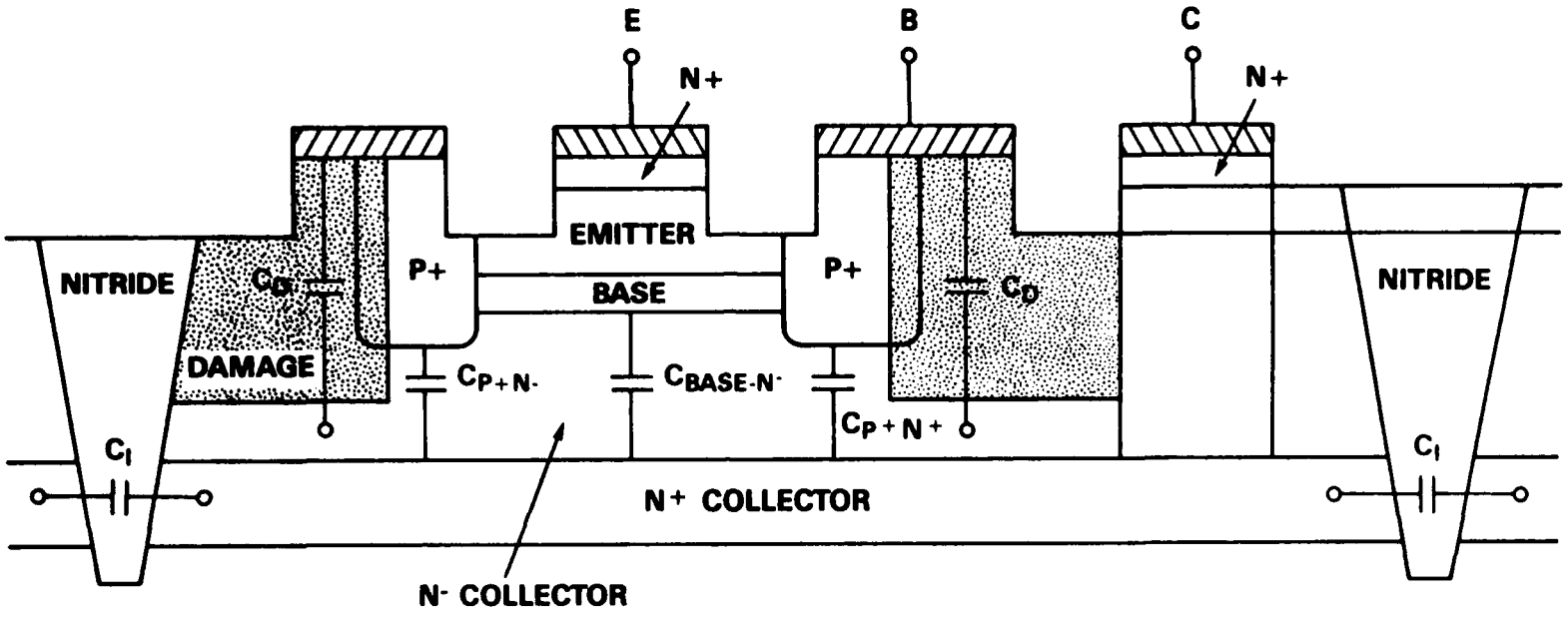
modifications were required to complete the upgrade since the old 7 x 7 μm^2 devices were replaced with a metal-1 compatible version of the new 5 x 5 μm^2 device. To minimize design time, power scaling of the 5 x 5 μm^2 5-bit ADC was not performed. A maximum clock frequency > 1 GHz is expected if the 5 x 5 μm^2 target device parameters are attained.

III. HETEROJUNCTION BIPOLAR PROCESS DEVELOPMENT

After careful measurements of the HBT parameters and comparison of these parameters with the HBT model used in the design, it became apparent that the lower-than-expected maximum operating frequency for the 5-bit HBT ADC was limited by greater-than-anticipated collector-to-base (C-B) capacitance. Measurements indicate that the actual capacitance was 2 to 2.5 times the anticipated value.

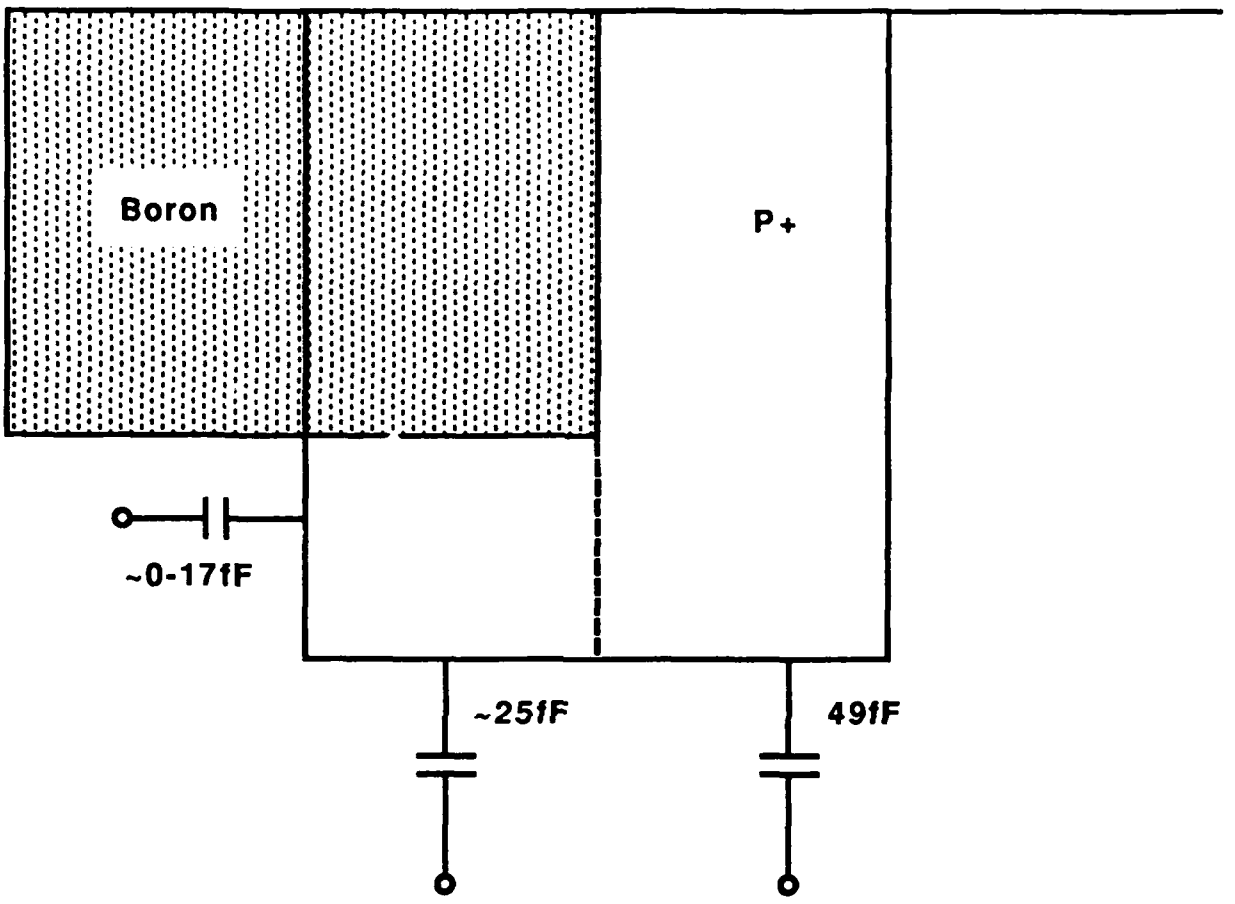
Process development efforts during the past quarter have been directed at determining the source of this discrepancy and its elimination. Figure 4 illustrates the cross section of the HBT and highlights the four identifiable capacitance components making up the C-B capacitance: C_D, the capacitance of the base contact metal overlapping the damage region; C_{P+N}, the capacitance of the extrinsic base region overlapping the N- collector; C_{BASE-N}, the intrinsic B-C capacitance; and C_I, the isolation capacitance between adjacent HBT collector regions. The fraction γ of C_I appearing across the collector-base electrodes depends on the details of the metal interconnect associated with the HBT.

The value C_D is determined by the area of the P-ohmic metal overlapping the damage region and the depth of the implant region. Based on LSS theory, the energy of the boron damaging implant was thought to be sufficient to result in the damage region extending completely through the extrinsic base contact region (Figure 4). It has been experimentally determined that this was not the case; instead, the beryllium implant that forms the P regions was being implanted deeper than the boron (Figure 5). This results not only in an increase in C_D because of a thinner-than-expected damage thickness, but also in a significant increase in the collector-to-extrinsic-base p-n junction area from 176 μm^2 to 297 μm^2, which increases C_{P+N} by 68%.



$$C_{BC} = C_D + C_{P+N} + C_{BASE-N} + \gamma C_I$$

Figure 4. Analysis of collector-base capacitance.



C_{BC}= 96 fF with complete boron isolation

C_{BC}~ 96 + 25 +~8 = 129 fF with incomplete isolation

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Figure 5. Analysis of collector-base capacitance: impact of incomplete boron damage.

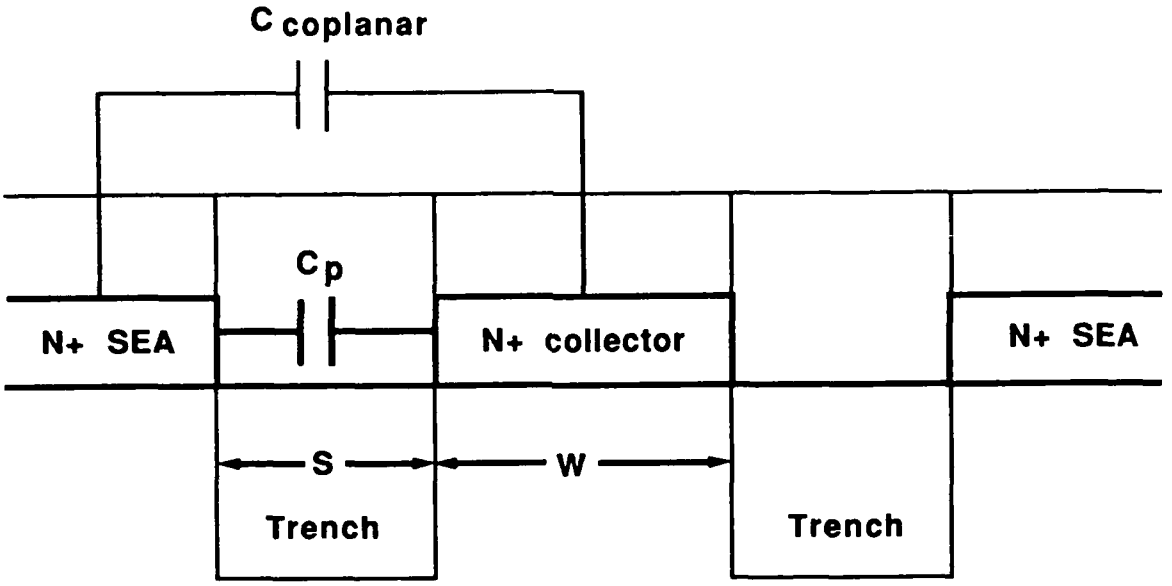
To experimentally verify that insufficient boron damage could account for the increased capacitance, a lot nearing completion was implanted using the standard boron process (5 x $10^{11}/cm^2$ at 40 keV and 9 x $10^{11}/cm^2$ at 120 keV). It was then re-implanted with boron at 8 x 10^{13} atoms/cm^2 and 200 keV. The completed lot was delivered to Hughes to measure the collector-to-base capacitance. The results are shown in Table 2:

Table 2
Comparison of C-B Capacitance for Different Boron Implants

Modeled Capacitance	63.5 fF
Measured Capacitance From Previous Lot (Lot 107) (Standard Boron Process)	170 fF
Measured Capacitance From Lot 112 With 8 x 10^{13} atoms/cm^2 at 200 keV boron implant	72 fF

Table 2 shows that the insufficient boron implant damage appears to account for the major contribution to the increased collector-to-base capacitance. Future lots will use both a modified boron implant process as well as a lower-energy beryllium implant to further reduce C_{P+N} for increased speeds.

Experimental capacitance measurements from large test transistors indicate that the measured intrinsic base capacitance C_{BASE-N} agrees well with the modeled value. Hence, this component has been eliminated as a problem. The capacitance C_I associated with the transistor-transistor isolation was not included in the original model. It is composed of two components, as indicated in Figure 6. The first is associated with the parallel plate capacitance formed from the collector cross-sectional area separated by the nitride used to refill the trench. The second component of C_I results from the coplanar capacitance of the HBT collector region



$$C_I = C_p + C_{coplanar}$$

$$C_p = \frac{\text{Transistor Perimeter} * \text{Epi Thickness}}{\text{Trench Width}} * \text{permittivity}$$

$$C_{coplanar} \simeq \frac{4W}{W + 2 * \text{Trench Width}} * \text{permittivity}$$

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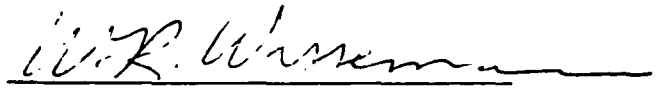
Figure 6. Analysis of collector-base capacitance isolation capacitance.

surrounded by a "sea" of N+ GaAs. To reduce C_I, it is necessary to increase the width of the trench or eliminate the N+ sea. Efforts are under way to eliminate the N+ sea by using a high-energy (4.5 MeV) oxygen implant to damage this region and convert it into semi-insulating GaAs.

IV. PLANS FOR NEXT QUARTER

1. Complete layout and release 12-bit ADC subcircuit test bar mask set.
2. Continue system and detailed circuit design of complete 12-bit ADC.
3. Demonstrate 5-bit ADC with >1 GHz maximum sampling frequency.



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